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Design of Low-Power CMOS Cell Structures Using Subthreshold Conduction Region

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Abstract— Subthreshold (leakage or cut-off) currents are a necessary evil in traditional VLSI design methodologies. These currents increase exponentially as threshold voltage scales, creating a serious problem for traditional design approaches. This work is based on the exclusive use of subthreshold conduction currents to perform circuit operations, turning this problem into an opportunity. It yields a dramatic improvement in power consumption compared to traditional circuit design approaches. This improvement makes it feasible to design extreme low-power circuits with such an approach. The CMOS digital circuits for this work have been designed using standard TSMC 0.18 *μm* Technology.

Index Terms—Low-Power, Leakage Current, Subthreshold Conduction.

1 Introduction

With the growing scale of integration, more and more sophisticated signal processing systems need to be implemented on a VLSI chip. For these signal processing applications, power consumption has become a critical concern in today's VLSI system design. The need for low-power VLSI systems arises from two main forces. First, with the steady growth of processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low-power design directly leads to prolonged operation time in these portable devices.

Also, with shrinking technology sizes, energy efficiency has become a critical aspect of designing digital circuits. Traditionally, voltage scaling, a mechanism in which the supply voltage is varying and the threshold voltage is constant, has been an effective solution in meeting stringent energy requirements. However, voltage scaling does come at a cost of reduction in performance. The limits of voltage scaling, and therefore energy minimization, can be explored by operating a circuit at subthreshold [1]. In subthreshold circuits, the supply voltage is reduced well below the threshold voltage of a transistor. Due to the quadratic reduction in power with respect to the supply voltage, subthreshold circuits are classified as *ultra low-power circuits*.

Specifically in application areas where performance can be sacrificed for low-power, subthreshold circuits are an ideal fit. Some of the applications include devices such as digital wrist watches, radio frequency identification (RFID), sensor nodes, pacemakers and battery operated devices such as, cellular phones.

2 Why To Reduce The Power

Up until now, the power consumption has not been of great concern because of the availability of large packages and other cooling techniques having the capability of dissipating the generated heat. However, continuously increasing density as well as the size of the chips and systems might cause to difficulty in providing adequate cooling and hence, might either add significant cost to the system or provide a limit on the amount of the functionality that can be provided [2].

Another factor that fuels the need for low-power chips is the increased market demand for portable consumer electronics powered by batteries. For these high performance portable digital systems, running on batteries such as-laptops, cellular phones and personal digital assistants (PDAs), low-power consumption is a prime concern because it directly affects the performance by having effects on battery longevity.

Hence, low-power VLSI design has assumed great importance as an active and rapidly developing field. Due to their extreme low-power consumption, subthrehsold design approaches are appealing for a widening class of applications which demand low-power consumption and can tolerate larger circuit delays.

3 Subthreshold Conduction For Low Power VLSI Design

In traditional digital VLSI design, the subthreshold region of operation is avoided, since it contributes toward leakage power consumption when the device is in standby. But the power can be reduced significantly by exclusively utilizing this subthreshold leakage current to implement circuits. This is achieved by actually setting the

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circuit power supply V_{dd} to a value less than or equal to V_{th}. The subthreshold current is exponentially related to gate voltage giving the exponential reduction in power consumption, but also an increase in circuit delay [3]. So, we use the circuits operating in subthreshold conduction region where the power is main concern and large delay can be tolerated.

The MOS transistor conducting below the threshold voltage V_{th} is called subthreshold conduction. Fig. 1 shows that the current I_d has linear dependency in the strong inversion region while in the moderate inversion region it shows quadratic dependency on gate voltage. The current in subthreshold conduction region changes exponentially, similar to BJT operation.

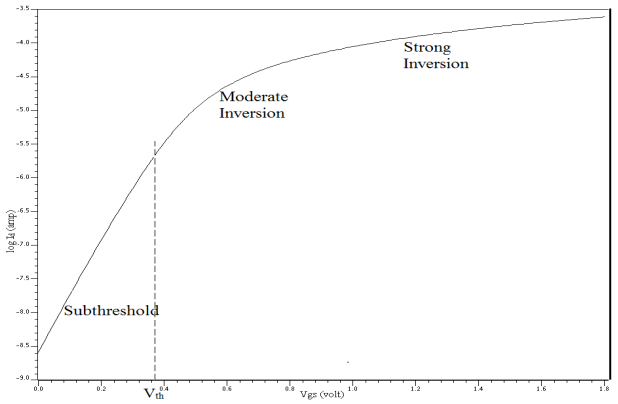

Fig. 1 CMOS Conduction region for an NMOS with V_{ds}= 1.8 V and V_{gs}varying from 0 V to 1.8 V.

Unlike moderate and strong inversion, in which the drift component of current dominates, subthreshold conduction is dominated by diffusion current [4].

3.1 Modelling of subthreshold current

In subthreshold conduction, the channel of the transistors is not inverted and current flows by diffusion. Subthreshold current can be expressed by the following basic equation:

$$I_{on-sub} = I_0 \, exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right) \quad (1)$$

Equation (2) shows the same basic equation with low V_{ds} roll-off:

$$I_{on-sub} = I_0 \, exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (2)$$

where I_0 is the drain current when V_{gs}= V_{th} given below:

$$I_0 = \mu_{eff} C_{ox} \frac{W}{L_{eff}} (n-1) V_T^2 \quad (3)$$

As expected for the diffusion current, (1) shows that I_{on-sub} depends exponentially on V_{gs}. Here, W is the width of the transistor, L_{eff} is the effective length, μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, n is the subthreshold slope factor $\left(n = 1 + \frac{C_d}{C_{ox}}\right)$, V_{th} is the transistor threshold voltage and V_T is the thermal voltage,V_T =*(kT/q)*.

4 Minimum Energy Point Model

In this section, we will discuss a closed form solution for the optimum V_{dd} and V_{th} for a given frequency and technology operating in the subthreshold region means (V_{dd} V_{th}).

The total energy per operation of a digital CMOS circuit consists of two components: switching and leakage energy [6]. Here, we will discuss in terms of an inverter.

Hence, total energy per operation can be expressed as:

$$E_{Total} = E_{SW} + E_L = V_{dd}^2 \left(C_{eff} + W_{eff} K C_g L_{DP} exp\left(\frac{-V_{dd}}{nV_T}\right)\right) \quad (4)$$

where, C_{eff} is the average effective switched capacitance per operation, K is a delay fitting parameter, C_g is the output capacitance of the inverter and L_{DP} is the depth of the critical path.

To define the V_{dd} at which the *minimum energy point* should occur, the derivative of (4) is taken with respect to V_{dd}, setting it equal to zero, and applying a number of rearrangements, we find:

$$\left(2 - \frac{V_{dd}}{nV_T}\right) exp\left(2 - \frac{V_{dd}}{nV_T}\right) = \frac{-2C_{eff}}{W_{eff} K C_g L_{DP}} exp(2) \quad (5)$$

Now according to Lambert function [5],

$$\text{If} \quad y = xe^x \text{, then } x = \text{lambert W}(y)$$

So, the analytical solution for $V_{dd,opt}$ from (5) is given as:

$$V_{dd,opt} = nV_T \left(2 - \text{lambert W}\left(\frac{-2C_{eff}}{W_{eff} K C_g L_{DP}} exp(2)\right)\right) \quad (6)$$

Also, we can find the optimum value of V_{th} = $V_{th,opt}$ for a given frequency f as:

$$V_{th,opt} = V_{dd,opt} - nV_T \, log_e\left(\frac{f K C_g L_{DP} V_{dd,opt}}{I_0}\right) \quad (7)$$

If the argument to the natural log in (7) exceeds 1, then the assumption of subthreshold operation no longer holds because $V_{th,opt}$ $V_{dd,opt}$. This constraint shows that there is a maximum achievable frequency for a given circuit in the subthreshold region [6].

Swanson and Meindl analysed the VTC of an inverter and showed that the inverter operation could be simulated down to 100 mV [7]. The VTC curves for different supply voltages for an inverter are shown in Fig. 2. To find the minimum voltage, Swanson equated the *off* current of NMOS and PMOS and calculated the inverter gain

in subthreshold. Since an inverter must have sufficient gain at $V_{dd}/2$, the minimum voltage which can be used was estimated to be 8(kT/q) or 0.2 V [7].

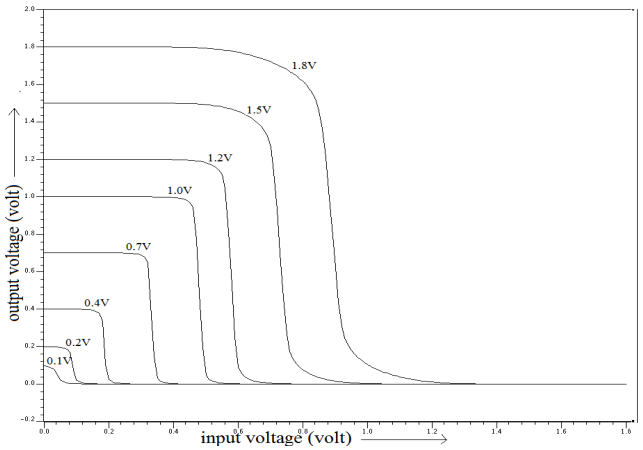

Fig. 2 Inverter VTC showing operation down to 100 mV in a 0.18 μm process.

5 Designing Of Different CMOS Cells

This section describes the design of various digital CMOS cells in subthreshold. First, the basic CMOS Inverter, shown in Fig. 3, is analyzed in detail and then, based on this analysis, the NAND and the NOR gates are designed and after that other circuits can also be designed by calculating the values of *W/L* with the help of these *W/L* values of Inverter which has been designed for symmetric output and equal charging and discharging current.

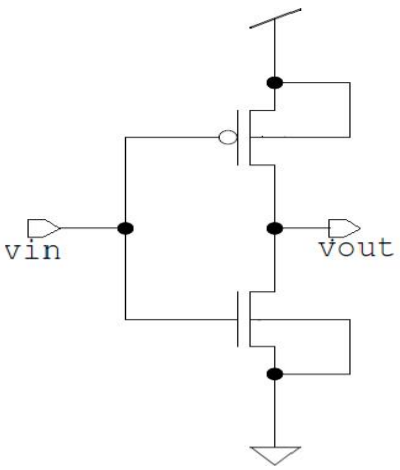

Fig. 3 Basic CMOS Inverter

By simulating this CMOS Inverter using TSMC 0.18 μm technology, the Inverter's values of *W/L* for PMOS = (1.2 μm/0.18 μm) and *W/L* for NMOS = (0.27 μm/0.18 μm) were obtained for strong inversion operation. While the Inverter's values of *W/L* for PMOS = (3.0 μm /0.18 μm) and *W/L* for NMOS = (0.27 μm/0.18 μm) were obtained for subthreshold operation.

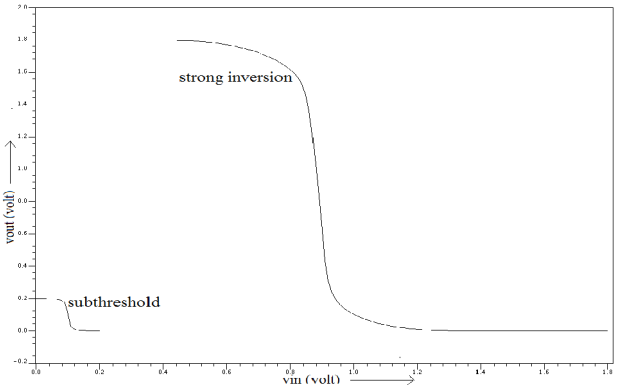

Fig. 4 VTC curves for Inverters operating in strong inversion and subthreshold.

By using these values of *W/L* of basic Inverter, other circuits can be designed having the equivalent *W/L* values equal to that of this basic Inverter.

6 Design And Simulation Results Of Different Cmos Circuits

6.1 CMOS Inverter

The load capacitance, for the inverter described in previous section, for strong inversion region is 5 *fF* while the load capacitance for subthreshold conduction is 11 *fF*.

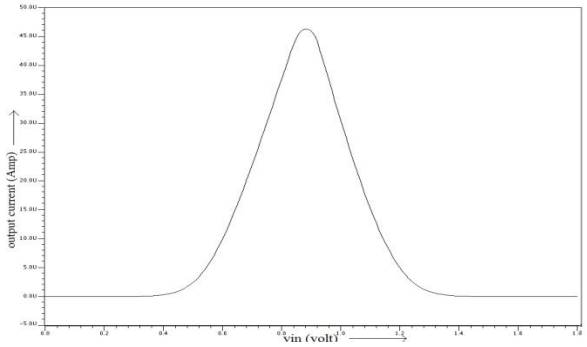

Fig. 5 Output current variation with input voltage in strong inversion region with V_{dd} = 1.8 V.

From Fig. 5 and 6, it is clear that the current depends on input (gate) voltage linearly in strong inversion region and exponentially in subthreshold region.

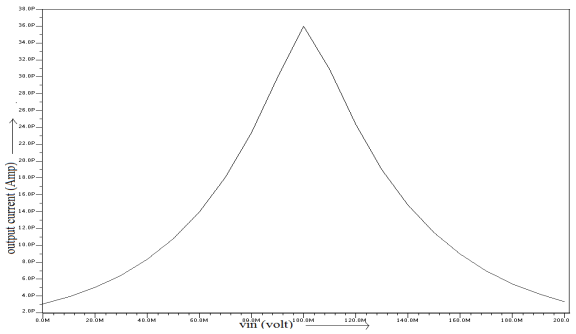

Fig. 6 Output current variation with input voltage in subthreshold region with V_{dd} = 0.2 V.

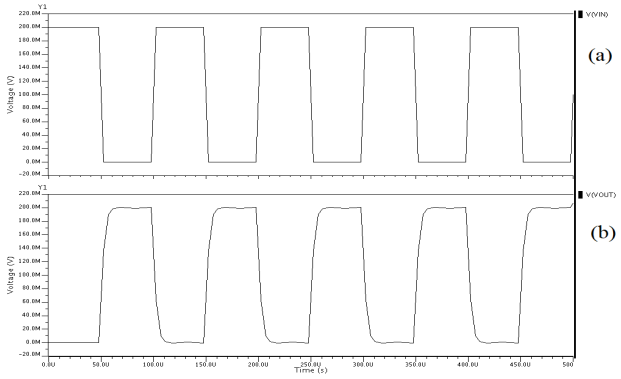

Fig. 7 Simulation result of transient analysis for CMOS Inverter in subthreshold region: (a) Input Signal, (b) Voltage waveform of Output Signal.

6.2 Two-input CMOS NAND Gate

Two-input CMOS NAND Gate can be designed having the equivalent *W*/*L* value equal to that of the Inverter.

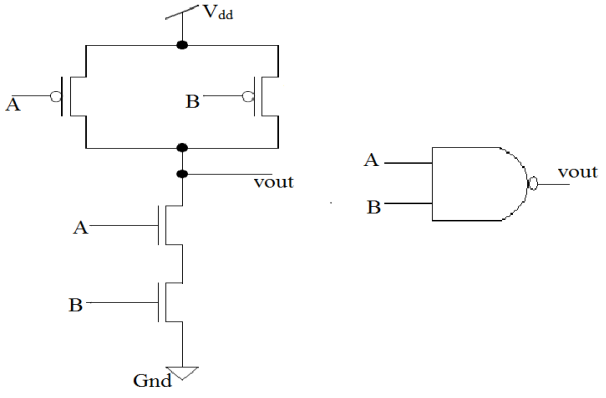

Fig. 8 Basic Structure of a 2-input CMOS NAND Gate

The load capacitance, for the NAND Gate designed, for strong inversion is 10 *fF* while for subthreshold conduction is 18 *fF*.

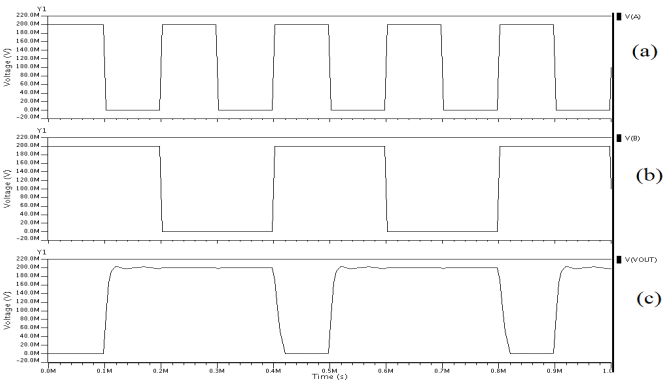

Fig. 9 Simulation result of transient analysis for a 2-input CMOS NAND Gate in subthreshold conduction region: (a) Input Signal (A), (b) Input Signal (B), (c) Voltage waveform of Output Signal (VOUT).

6.3 Two-to-One CMOS Multiplexer

The basic structure and its simulation result of a 2-to-1 CMOS Multiplexer are shown in Fig. 10 and 11.

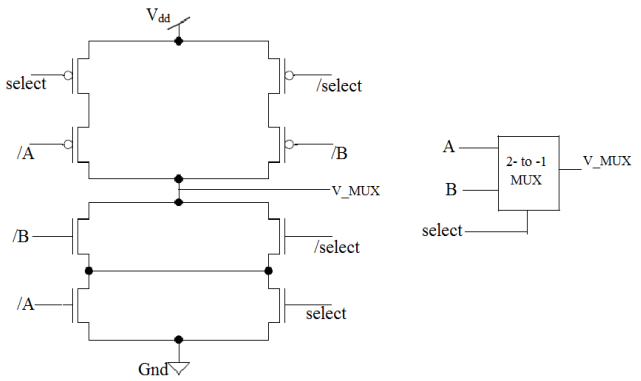

Fig. 10 Basic Structure of a 2-to-1 CMOS Multiplexer

The load capacitance, for the 2-to-1 CMOS Multiplexer designed, for strong inversion is 13 *fF* while for subthreshold conduction is 30 *fF*.

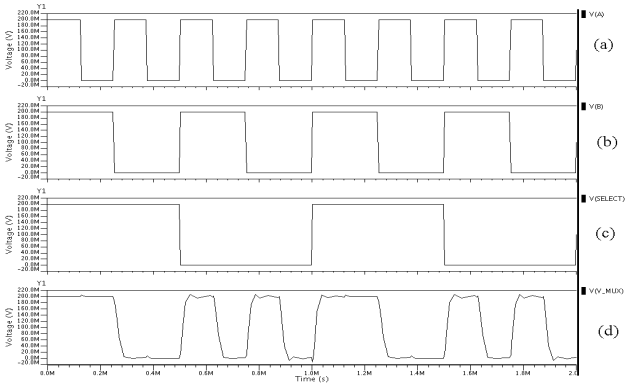

Fig. 11 Simulation result of transient analysis for a 2-to-1 CMOS Multiplexer in subthreshold conduction region: (a) Input Signal (A), (b) Input Signal (B), (c) Input Signal (SELECT) (d) Voltage waveform of Output Signal (V_MUX).

6.4 One-Bit CMOS Full Adder

Full Adder is basic structure for any arithmetic circuit, so the design of a Full Adder is also necessary. The basic

structure and simulation result for a One-Bit CMOS Full Adder are shown in figures given below.

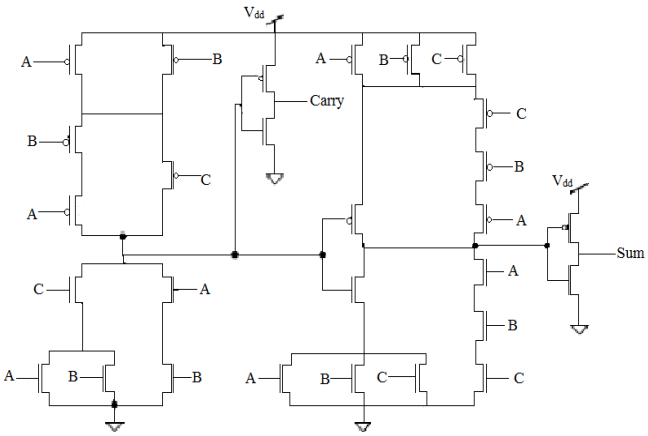

Fig. 12 Basic Structure of a One-Bit CMOS Full Adder

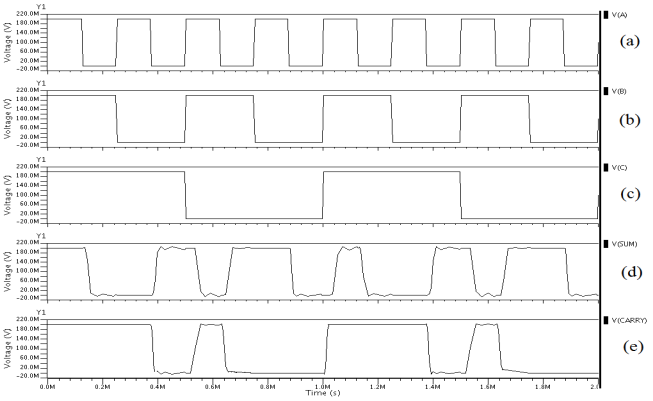

Fig. 13 Simulation result of transient analysis for a One-Bit CMOS Full Adder in subthreshold conduction region: (a) Input Signal (A), (b) Input Signal (B), (c) Input Signal (C), (d) Voltage waveform of Output (SUM) Signal, (e) Voltage waveform of Output (CARRY) Signal.

TABLE I
POWER DISSIPATION IN DIFFERENT CMOS CIRCUITS

		Power (nW)	
		f = 4 kHz	*f* = 5 kHz
CMOS Inverter	Superthreshold	389.54 n	486.93 n
	Subthreshold	0.002107 n	0.002576 n
2-input NAND	Superthreshold	366.56 n	442.54 n
	Subthreshold	0.002732 n	0.003382 n
2:1 MUX	Superthreshold	869.55 n	1038.58 n
	Subthreshold	0.004995 n	0.005414 n
Full Adder	Superthreshold	971.15 n	1100.94 n
	Subthreshold	0.024413 n	0.027932 n

Fig. 14 shows the dynamic power variation with different clock frequencies for a 1-bit Full Adder operating in subthreshold conduction region.

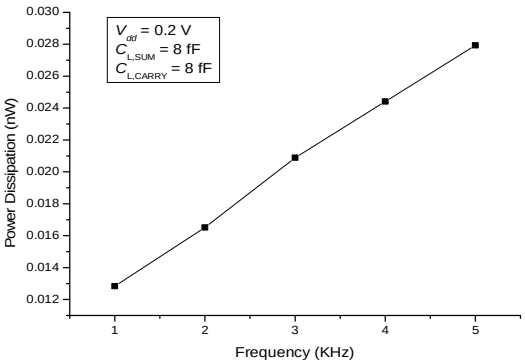

Fig. 14 Power dissipation results for a 1-bit Full Adder operating in subthreshold conduction region.

7 LAYOUT DESIGN AND POST-LAYOUT SIMULATION RESULT FOR A 1-BIT CMOS FULL ADDER

For a 1-bit Full Adder operating in subthreshold conduction resgion, layout and post-layout simulation results are shown in Fig. 15 and 16 respectively.

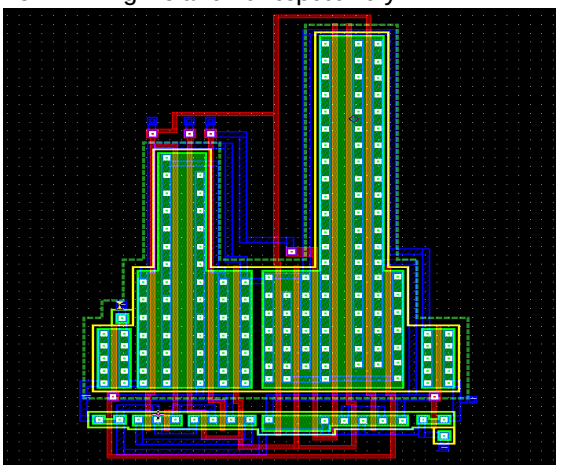

Fig. 15 Layout of 1-bit CMOS Full Adder operating in subthreshold conduction region.

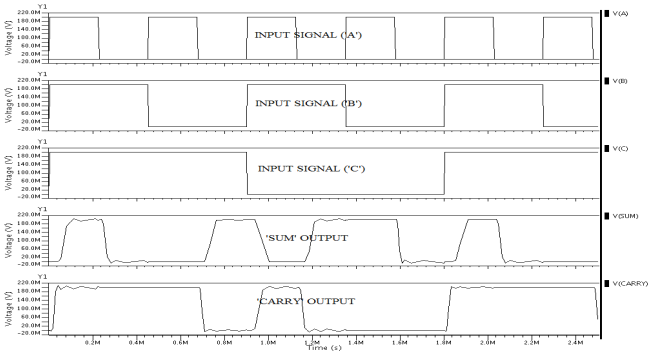

Fig. 16 Post-Layout Simulation – Transient analysis for 1-bit CMOS Full Adder operating in subthreshold conuction region.

8 CONCLUSIONS

Based on the subthreshold conduction, the designing of various digital circuits have been done. The supply voltage used for the circuits operating in subthreshold conduction region is 0.2 V. The power analysis also has been carried out for the circuits, operating in subthreshold conduction region and in superthreshold conduction region. It is found that the circuits operating in subthreshold conduction region provide the significant power reduction than the superthreshold conduction region.

It can be found that subthreshold conduction region is advantageous in applications where power is the main concern and performance can be sacrificed to achieve the low-power because the speed of a circuit operating in subthreshold conduction region becomes significantly slow.

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